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RICHARD JAWORSKI
COOPER & DUNHAM LLP
1185 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	11

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/469,754	Applicant(s) TSUKAMOTO ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-39 have been presented for reconsideration in light of Applicant's terminal disclaimer and amended claim language.

Response to Arguments

2. Applicant's arguments filed on 22 September 2003 have been fully considered. Examiners response is as follow:

2.1 Regarding applicants response to Examiners rejection of Claims 25-32, 33-36, 39, 1-8, 17-24 and 38 under the judicially created doctrine of obviousness-type double patenting:

Applicants have argued that:

> Claims 25-32 were rejected under the judicially created doctrine of obviousness -type double patenting as allegedly unpatentable over claim 4 of U.S. Patent No. 6,094,527. Claims 33-36 and 39 were rejected under the judicially created doctrine of obviousness -type double patenting as purportedly unpatentable over claim 6 of U.S. Patent No. 6,094,527. Claims 1-8 were rejected under the judicially created doctrine of obviousness -type double patenting over claim 1 of U.S. Patent No. 6,094,527. Claims 17-24 were rejected under the judicially created doctrine of obviousness -type double patenting as allegedly unpatentable over claim 3 of U.S. Patent No. 6,094,527. Claims 9-16 were rejected under the judicially created doctrine of obviousness -type double patenting as allegedly unpatentable over claim 2 of U.S. Patent No. 6,094,527. Claim 38 was rejected under the judicially created doctrine of obviousness -type double patenting as allegedly unpatentable over claim 4 of U.S. Patent No. 6,094,527.
> Applicants submit concurrently herewith a Terminal Disclaimer.
>
> Accordingly, Applicants respectfully request that the rejections under the judicially-created doctrine of obviousness type double-patent be withdrawn.

The Examiner thanks the Applicant for sending in a terminal disclaimer and withdraws the earlier rejections of Claims 25-32, 33-36, 39, 1-8, 17-24 and 38 under the Judicially created doctrine of obviousness-type double patenting.

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must comply with 37 CFR 3.73(b).

2.2 Regarding applicants response to the 35 U.S.C. 101 rejection of Claims 1-39:

Applicants have argued that:

> Claims 1-39 were rejected under 35 U.S.C. §101 as allegedly lacking utility and under 35 U.S.C. §112, first paragraph. According to the Office Action, the stored executable code as recited in the claims is not actually executed. In response, without conceding the correctness of the Examiner's position, but solely to advance prosecution of the subject application, the claims have been amended to clarify the subject matter Applicants claim as the invention and to place the claims in better form for examination, without narrowing the scope of the claims.
>
> Accordingly, withdrawal of the rejections under 35 U.S.C. §101 and under 35 U.S.C. §112, first paragraph is respectfully requested.

The Examiner asserts that the amended claims language to the claims that were rejected under 35 U.S.C. 101 has now overcome that earlier rejection and the claims are now directed towards statutory subject matter.

From the MPEP: Chapter 700, Patentable Subject Matter—Computer-related Inventions:

> Apart from the utility requirement of 35 U.S.C. 101, usefulness under the patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement. See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole

must produce a "useful, concrete and tangible" result to have a practical application.

The Examiner asserts that while the scope of the original claims remains unchanged, the Examiner was correct, as disclosed in the preceding section of the MPEP in rejecting those claims, that in their original form, where not directed towards statutory subject matter. The earlier 35 U.S.C. 101 and 35 U.S.C. 112 rejections of Claims 1-39 are withdrawn.

2.3 Regarding the Applicant's response to the 35 U.S.C. 103 rejections of claims 1-39:

The Applicants have argued:

> Claims 1-39 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent 5,943,487 to Messerman et al. in view of U.S. Patent No. 6,324,678 to Dangelo et al. ("Dangelo '678"), and further in view of U.S. Patent No. 5,867,397 to Koza et al., and further in view of the Microsoft Press Computer Dictionary, Third Edition. Claims 1-39 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,535,370 to Raman et al. in view of U.S. Patent No. 5,521,834 to Crafts et al. and further in view of U.S. Patent No. 5,493,508 to Dangelo et al. ("Dangelo '508"). Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claims 1, 9, 17, 25, 29, 33, and 37-39 are patentable over the cited art, for at least the following reasons.
>
> The present application relates to estimating power consumption of an integrated circuit. As portable electronic devices proliferate through our society, an accurate estimation of power consumption by the devices is often desired during the design and simulation stage. As discussed in the application at pages 1-2, conventional methods of estimating power consumed by integrated circuits include (1) determining, from logic simulations, the number of operation events at terminals or pins of each basic Cell and estimating power consumption based on the number of events and pre-established power consumption data, or (2) estimating power consumption based on collected information for each basic cell regarding changes over time in output voltage signals, program instructions for the operation modes, and power consumption by the basic cells. The conventional methods, however, do not accurately estimate power consumption for integrated circuits.
>
> Applicants found that power consumption by integrated circuits may be more accurately estimated by using information collected during

logic simulation to estimate current consumed by mega cells and current consumed by basic cells.

For example, each of independent claims 1 and 9 relates to a computer readable medium including computer executable code stored thereon. According to claim 1, the code is executable by a processor to perform a method for estimating power consumption of an integrated circuit which includes (a) simulating logic of basic and mega cells of the integrated circuit, (b) estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, (c) estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and (d) combining the first and second values to obtain the power consumption of the integrated circuit.

According to claim 9, the code is executable by a processor to perform a method for estimating electric power consumed by basic cells and mega cells of an integrated circuit to estimate total power consumed by the integrated circuit which includes simulating logic of said basic cells and said mega cells, wherein each function of each mega cell for logic simulation is defined by hardware description language, estimating a current consumed by the basic cells for estimating a first value of electric power consumed by said basic cells based on logic simulation results from said logic simulations and pre-established power consumption data for each logic state of each input and output terminal of said basic cells, estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate said current consumed by the mega cells for estimating a second value of electric power consumed by said mega cells based on logic simulation results from said logic simulations and pre-established power consumption data for said logic states, variables in the function description, and said operating frequencies at each input and output terminal of each mega cell, and adding said first and said second values of the power consumption to determine the total power consumption for the integrated circuit. Messerman, as understood by Applicants, relates to extraction of a resistor network from an integrated circuit polygon layout. Operation of the resistor network is simulated to perform electromigration (which is the motion of ions through a conductor in response to the passage of current through the conductor) analysis, the results of which can then be used to estimate the reliability of the integrated circuit.

As acknowledged in the Office Action, Messerman, which is cited as a primary reference, does not disclose or suggest several aspects of the claimed invention.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It is the combination of references that are used to teach the Applicants claimed invention. The rejections do not rely only on a single reference to teach the Applicants claimed invention but on the combinations of the references.

> However, the Office Action cites Messerman, column 1, line 12 through column 2, line 46, and column 7, lines 44-63, as alleged support that Messerman discloses code for estimating electric power consumed by the resistor network and pre-established power consumption data and code for determining the power consumption of the integrated circuit's resistor network. Applicants respectfully disagree. Messerman, column 1, line 12 through column 2, line 46 discloses conventional techniques for extracting a resistor network from a symbolic layout of an integrated circuit, and using the resistor network to analyze electromigration within the circuitry of the integrated circuit. Messerman, column 7, lines 44-63, discloses a sequence of steps for identifying electromigration violations and generating a composite map of the electromigration violations.
>
> Applicants find no teaching or suggestion in Messerman of a method for estimating electric power consumed by basic cells and mega cells of an integrated circuit to estimate total power consumed by the integrated circuit.
>
> Accordingly, Applicants maintain that it would not have been obvious to one of ordinary skilled in the art to make any combination of the references, which includes Messerman as a starting point, without using the claimed invention as a roadmap in impermissible hindsight for piecing together the disclosures of the cited references. Furthermore, Applicants submit that one looking to devise a technique for estimating electric power consumed by basic cells and mega cells of an integrated circuit to estimate total power consumed by the integrated circuit would not have looked to the teachings of Messerman, since the reference does not purport to provide teachings in that field.

The Examiner asserts that for teaching the limitation of mega-cell and basic cells power consumption the 35 U.S.C. 103 rejections relied on the combination with the *Dangelo et al.*

reference (U.S. Patent 6,324,678). In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The Examiner asserts that the Applicants has implied that the *Messerman et al.* reference (U.S. Patent 5,943,487) is non-analogous art. The Examiner asserts that the *Messerman et al.* reference is directed towards calculation of power consumption as disclosed in **(Col. 1 lines 34-45),** specifically, the *Messerman et al.* reference teaches, "Resistor networks are typically extended from the symbolic layout of an IC solely for the purpose of simulating the electrical characteristics of the IC." The Examiner asserts that power consumption is an electrical characteristic of an IC.

> Dangelo '678, as understood by Applicants, relates to methodologies for deriving a valid structural description of a circuit or system (i.e. device) from a behavioral description thereof. Typically, a designer specifies the desired behavior of the device in a high-level language, such as VHDL. The description includes high-level timing goals. Next, starting with the VHDL behavioral description of a design, the designer iterates through simulation and design changes until the desired behavior is obtained. Next, the design is partitioned into a number of architectural blocks.
>
> Dangelo '678, column 36, line 35 through column 41, line 52, discloses techniques for estimating power consumption in integrated circuits which includes two parts: static power consumption and dynamic power consumption. Static power dissipation is calculated by multiplying, for each logic device or gate in the circuit, a leakage current (i.e. a static current draw) of the device and a supply voltage, and summing the products for the entire collection of logic devices in the circuit. Dynamic power dissipation for a CMOS device is calculated using output load capacitance, supply voltage, clock cycle, and the number of switching transitions per clock cycle as parameters. However, Applicants find no teaching or suggestion in Dangelo of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic

> simulations and pre-established power consumption data, estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and combining the first and second values to obtain the power consumption of the integrated circuit.

The Examiner asserts that by Applicants own admission the *Dangelo et al.* reference discloses calculation of power consumption in an mega-cells and basic cells. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The *Deangelo et al.* reference discloses logic simulation **(Figure 8 "VHDL SIMULATOR", Figure 9 Item 904),** and Power estimation **(Figure 18 ITEM 1896, Col. 3 Lines 26-34).** It is noted by the Examiner that the *Koza et al.* reference was relied upon for the rejections of the following claim limitations, *determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component*, and *estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and combining the first and second values to obtain the power consumption of the integrated circuit.*

> Koza, as understood by Applicants, relates to automated design of complex structures (such as circuits) using genetic algorithms. The behavior of the developed structure is determined, compared to the predetermined design goals and then evolved until it meets the design goals. Simulations and fitness measures as discussed in Koza focus solely on circuit behavior in terms of inputs and outputs. Koza is cited in the Office Action as purportedly disclosing measuring alternating current of logic cells.

The Examiner asserts that the calculation of alternating current components and direct current components of circuits in integrated circuits is known in the art as disclosed in the *Koza et al.* reference. The *Koza et al.* reference was relied upon to teach those specific claim limitations of calculating/measuring the alternating current of logic cells and the ability to perform the calculation/measurement of alternating current is known in the electrical engineering art. The *Koza* reference discloses, determining an alternating current component and a direct current component for each logic state to calculate the current consumed, **(Note VSOURCE in Figure 35, this is the "~" symbol is for alternating current).**

> Microsoft Press Computer Dictionary is cited in the Office Action as disclosing use of various computer readable media.

The use of computer readable media for storing executable code on a processor is known in the computer art as disclosed in the *Microsoft* reference.

> However, Applicants find no teaching or suggestion in the cited art of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit which includes (a) simulating logic of basic and mega cells of the integrated circuit, (b) estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, (c) estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and (d) combining the first and second values to obtain the power consumption of the integrated circuit, as recited in independent claim 1.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

> Raman, as understood by Applicants, relates to current and power consumption analysis of a circuit through simulation with a model of the circuit. According to Raman, input test vectors are used to drive the model, and a simulator which operates the model maintains a toggle count for each device of the circuit. A characterization table is generated which contains an average switching current value of a type of a device for different values of capacitive loads. An activity factor can then be generated based on the number of the toggle count during a sample time period and the number of clock cycles during the sample period. Using the activity period, the current is determined from the average switching current-, for the device times the activity factor. The current can then be used to perform such calculations as power consumption and electromigration testing.
>
> The Office Action acknowledges that Raman does not disclose or suggest mega cells and calculating the alternating current component for each cell.
>
> In addition, Applicants find no teaching or suggestion in Raman of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references and that is why the *Dangelo et al.* reference is used in the rejection of the limitation of the mega-cells and the *Crafts et al.* reference is relied upon to teach the determination of the alternating current calculation. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Examiner asserts that the *Dangelo et al.* and *Crafts* references were relied upon to teach the express deficiencies of the *Raman* reference.

> Crafts, as understood by Applicants, relates to techniques for approximating power dissipation of CMOS circuits. A determination is made of the capacitive load for each cell in a netlist for the CMOS

> circuit, from cell library data sheets, and the capacitive loads of the interconnects between stages are estimated. A switching rate for each cell is then calculated using one of two alternative methods. The first method assumes that the patterns of input signals are statistically independent, and thus estimates the switching rate from the structure of the cell and the switching rates of the inputs. The second method uses known information concerning the relative times when the input signals are high or low to determine the switching rate of the cell. Once the switching rate is known, the output frequency for the cell can be determined. The power dissipation for each cell is then calculated by multiplying the output frequency by the capacitive load. The dynamic power dissipation for the circuit is determined by summing the power dissipation terms for each of the cells making up the netlist.

Switching rate is the rate at which the circuit is *alternating* from one state to another state. The Examiner asserts that the *Crafts* reference is teaching the limitation of calculating the frequency for a particular logic circuit and the calculation of power dissipation, if we know the power dissipation and the frequency then the current calculation is derived. These methods are known in the Electrical Engineering art and are inherent to the *Crafts* reference.

> Crafts was cited in the Office Action as purportedly disclosing calculating the alternating current component for each cell.
> However, Applicants find no teaching or suggestion in Crafts of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references and that is why the *Dangelo et al.* reference is used in the rejection of the limitation of the mega-cells and the *Crafts et al.* reference is relied upon to teach the determination of the alternating current calculation. The *Crafts et al.* reference teaches the calculation of alternating and direct current in figure 2 where the block labeled 34 states "Calculate Power Dissipation", it is known in the Electrical Engineering art that to calculate

power dissipation you need to calculate the current. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

> Dangelo '508, as understood by Applicants, relates to generating structural descriptions of complex digital devices from high-level descriptions and specifications. Dangelo '508 was cited in the Office Action as purportedly disclosing mega cells and hardware description languages.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *See* In re Keller, *642 F.2d 413, 208 USPQ 871 (CCPA 1981);* In re Merck & Co., *800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).* The Examiner asserts that the combination of the *Raman et al.* U.S. Patent 5,535,370 reference, *Crafts et al.* reference U.S. Patent 5,521,834 and the *Dangelo et al.* U.S. Patent 5,493,508 reference.

> However, Applicants simply does not find teaching or suggestion in the cited art of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit which includes estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, as recited in independent claim 1.

The Examiner asserts that the cited references teach the claimed limitations using a reasonable interpretation of the claim language. The Examiner asserts that the cited references were properly combined and that the Applicant has not argued that combination of references. The Examiner has found the Applicant's arguments to be unpersuasive and uphold that earlier 35 U.S.C. 103(a) rejections of claims 1-39.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Messerman et al. U.S. Patent 5,943,487** in view of **Dangelo et al U.S. Patent 6,324,678** and in further view of **Koza et al. U.S. Patent 5,867,397** and in further view "**Microsoft Press Computer Dictionary, Third Edition, *Published 1997*** here after referred to as the *Microsoft* reference.

3.1 As regards **Claims 1, 25, 29 and 37** the *Messerman et al.* reference teaches the following limitations; A computer readable medium including executable code stored thereon, **(Figure 9 Items 410, 408 and 404),** code for simulating logic of an integrated circuit **(Figures 1-9 and Col. 1 Lines 46-58),** determining the direct current component for resistor network **(Col. 1 Lines 34-67 and Col. 2 Lines 1-8)**, code for estimating a current consumed by the resistor network for estimating a second value of electric power consumed by the resistor network and

pre-established power consumption data and code for combining said first and second values to obtain the power consumption of the integrated circuit's resistor network **(Col. 1 Lines 12-67 and Col. 2 Lines 1-46 and Col. 7 Lines 44-63).**

The limitations not expressly disclosed in the *Messerman et al.* reference are, code for simulating logic of basic and mega cells of the integrated circuit, determining the average frequency of operation for each logic state, determining the alternating current component for each logic state consumed by the mega cell.

The *Dangelo et al.* reference teaches code for simulating logic of basic and mega cells of the integrated circuit, **(Figure 1 Item 116 and Figure 8 Items 824 as regards logic see Figure 12 Items 1214 and 1226, and mega-cells Col. 44 Lines 47-61)**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Dangelo et al.* reference because, *motivation to combine*, the *Dangelo et al.* reference discloses simulation of logic circuits as well as power estimation ***(Col. 36 Lines 35 –67and Col. 37 Lines 1-67 and Col. 38 Lines 1-9 and Col. 39 Lines 18-67 and Col. 40 Lines 1-67 and Col. 41 Lines 1-52).***

The *Koza et al.* reference discloses measuring the alternating current of each logic cell, **(Note VSOURCE in Figures 25-35 and VSOURCE in Figures 53-61 also note the Z terms in Figures 53-56, these relate to frequency dependent elements in the circuit, Note Figures 82-85, Note Figure 105, Note Figures 108 Item OR6 and Figure 107 Item AND6 and Col. 16 Lines 13-39).** *Examiners Note: As regards the Koza et al. reference to being analogous art Examiner points out that this reference was issued in the 703/14 subclass entitled, "Simulating*

Electronic Device or Electrical System/Circuit simulation" a mega-cell in an ASIC or FPGA is an electronic device.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Koza et al.* reference because *(Motivation to combine)* by modeling the AC characteristics of each logic cell the designer is able to determine the fitness of each sub-circuit for its intended use ***(Koza et al. Col. 82 Lines 37-67 and Col. 83 lines 1-35).***

3.2 As regards **Claims 9 and 38,** the *Messermann et al.* reference does not expressly disclose a Hardware Description Language.

The *Dangelo et al.* reference discloses a hardware description language as well as a computer system for simulating mega cells, **(Figure 8 item 604, all of Figure 9, all of Figure 10, 11, 12, 13, 18 and 19, and Col. 1 Lines 25-67 and all of Columns 3, 4. and Col. 5 Lines 1-36, Col. 8 Lines 38-67 and Col. 9-18 and Col. 19 Lines 1-57.)**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Dangelo et al.* reference because, *motivation to combine*, the *Dangelo et al.* reference discloses simulation of logic circuits as well as power estimation ***(Col. 36 Lines 35 –67and Col. 37 Lines 1-67 and Col. 38 Lines 1-9 and Col. 39 Lines 18-67 and Col. 40 Lines 1-67 and Col. 41 Lines 1-52).***

3.3 As regards **Claims 17, 33 and 39,** the *Messermann et al.* reference does not expressly disclose compiling a table that tabulates data.

The *Dangelo et al.* reference discloses a compiling a table that tabulates data as well as a computer system for simulating mega cells, **(Figures 16a-b and Col. 5 Lines 56-63).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Dangelo et al.* reference because, *motivation to combine*, the *Dangelo et al.* reference discloses simulation of logic circuits as well as power estimation ***(Col. 36 Lines 35 –67and Col. 37 Lines 1-67 and Col. 38 Lines 1-9 and Col. 39 Lines 18-67 and Col. 40 Lines 1-67 and Col. 41 Lines 1-52).***

3.4 As regards **Claims 2-8, and 10-16 and 18-24** the previous rejections disclosed above address all of the limitations for **Claims 1, 9 and 17.**

3.5 As regards **Claim 2, 10 and 18,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a floppy disk.

The *Microsoft* reference discloses the use of a floppy disk **(Page 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the floppy disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

3.6 As regards **Claim 3, 11 and 19,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a 3.5-inch floppy disk.

The *Microsoft* reference discloses the use of a 3.5-inch floppy disk **(Page 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the 3.5-inch floppy disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

3.7 As regards **Claim 4, 12 and 20,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a compact disk.

The *Microsoft* reference discloses the use of a compact disk **(Page 82).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the compact disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

3.8 As regards **Claim 5, 13 and 21,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a read-only compact disk.

The *Microsoft* reference discloses the use of a read-only compact disk **(Page 82).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the compact disk is a known computer readable medium and by storing the program code on a

computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

3.9 As regards **Claim 6, 14 and 22,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a read/write compact disk.

The *Microsoft* reference discloses the use of a read/write compact disk **CD-R (Pages 81, 82).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the compact disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

3.10 As regards **Claim 7, 15 and 23,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a DVD.

The *Microsoft* reference discloses the use of a **DVD (Pages 145-146).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the DVD is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

3.11 As regards **Claim 8, 16 and 24,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of computer executable code that is compressed and non-compressed.

The *Microsoft* reference discloses the use of computer executable code **(Pages 182-183)** and compressed data **(Page 107)**.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because by compressing the computer executable code less storage space is required on the computer readable medium.

3.12 As regards **Claims 26, 30 and 34,** the *Messerman et al.* reference discloses a programmable computer in comprising a read/write unit in which a computer readable media including computer executable code can be input, the computer executable code being downloaded from the computer readable media via the read/write unit for execution by the processor **(Figure 9)**.

3.13 As regards **Claims 27, 31 and 35**, a programmable computer wherein the computer executable code is stored on computer readable media is discloses in **(Figure 9)** of the *Messerman et al.* reference.

However the *Messerman et al.* reference does not expressly disclose the executable code on the computer readable medium being in compressed format and is decompressed and downloaded to the storage media.

The *Microsoft* reference discloses executable code **(Page 182,183)** and a compressed format **(Page 107)**.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because, by compressing the executable code, storage space is conserved on the computer readable medium.

3.14 As regards **Claims 28, 32 and 36** the *Messerman et al.* reference discloses a programmable computer with a computer readable medium **(Figure 9).**

The *Messerman et al.* reference does not disclose at least one of a floppy disk, a CD, DVD and an Internet server.

The *Microsoft* reference discloses, a floppy disk **(Page 201)** a CD *or Compact Disk* **(Pages 81-82)** a DVD **(Pages 145 and 146)** and an Internet server **(Page 430).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because by storing the computer executable code on various computer readable medium the computer user does not need to re-enter the program code each time the code needs to be run and by using an internet server the program code can be accessed by any computer connected to the internet.

Note to the Applicant, the examiner has disclosed examples in each of the references that disclose the elements in applicant's claim for invention, the examiner directs the attention of Applicant to the Abstract, Backround of the Invention, Preferred embodiment, and Claims of the references sited.

4. **Claims 1- 39** are rejected under 35 U.S.C. 103(a) as being unpatentable in view of **Raman et al. U.S. Patent 5,535,370** in view of **Crafts et al. U.S. Patent 5,521,834** and in further view of **Dangelo et al. U.S. Patent 5,493,508.**

4.1 As regards **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** the *Raman et al.* reference discloses a method of calculation of power using a circuit simulation **(Figures 1-3),** using a lookup table with pre-established power consumption data **(Figure 1 Item 50, Col. 4 Lines 59-65),** for each logic state **(Figures 4(a), 4(b))**, determining the average operation frequency **(Figure 1 Item 20, Col. 1 Lines 50-64),** determining a direct current for each node **(Figure 3 Item 220, Figures 4(c) and 4(d), 6b, 7, Col. 1 Lines 65-67, Col. 2 Lines 1-31),** basic cells **(Col. 4 Lines 66-67, Col. 5 Lines 1-52),** and portions of a mega cell **(Col. 6 Lines 56-67, Col. 7 Lines 1-4).**

The *Ramen et al.* reference does not expressly disclose calculating the alternating current component for each cell.

The *Crafts et al.* reference discloses calculating the alternating current component for each cell **(Figure 2 Items 30, 32, 34, Col. 4 Lines 1-67, Col. 5 Lines 1-10).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Ramen et al.* reference with the *Crafts et al.* reference because, *(motivation to combine)* the *Crafts et al.* reference discloses a better approach that is more accurate to calculate the power dissipated in a CMOS IC *(Crafts et al. Col. 6 Lines 31-62).*

The *Ramen et al.* reference does not expressly disclose mega-cells and hardware description languages.

The *Dangelo et al.* reference discloses mega-cells **(Col. 11 Lines 1-4),** and hardware description languages **(Col. 11 Lines 49-55).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention to have modified the *Ramen et al.* reference with the *Dangelo et al.* reference because, *(motivation to combine)* the *Dangelo et al.* reference discloses an improved method of simulating mega-cells with a hardware description language *(Dangelo et al. Col. 4 Lines 13-67).*

4.2 As regards independent **Claims 25, 29, 30, 33, 34, 37, 38 and 39** the *Ramen et al.* reference does not expressly disclose a programmable computer.

The *Craft et al.* reference discloses a programmable computer **(Figure 1).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Ramen et al.* reference with the *Crafts et al.* reference because, *(motivation to combine)* the *Crafts et al.* reference discloses a better approach that is more accurate to calculate the power dissipated in a CMOS IC *(Crafts et al. Col. 6 Lines 31-62).*

4.3 As regards independent **Claims 1, 9 and 17** the *Ramen et al.* reference does not expressly disclose a computer readable medium with computer executable code.

The *Dangelo et al.* reference discloses a computer readable medium with computer executable code **(Col. 8 Lines 47-67).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention to have modified the *Ramen et al.* reference with the *Dangelo et al.* reference because, *(motivation to combine)* the *Dangelo et al.* reference discloses an improved method of simulating mega-cells with a hardware description language *(Dangelo et al. Col. 4 Lines 13-67).*

Conclusion

5. **Claims 1-39** are rejected under 35 U.S.C. 103(a),

5.1 **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
December 13, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER